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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,034	MITBANDER ET AL.	
	Examiner	Art Unit	
	John P. Trimmings	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003 and 21 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) *4,5,17 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/28/04, 6/20/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the applicant's submissions dated 12/31/2003 (the application date), 7/28/2004 (an IDS date), 6/20/2005 (an IDS date) and 9/21/2006 (a preliminary amendment).

Claims 1-23 are presented for examination.

Information Disclosure Statement

1. The examiner has considered the applicant's IDS's dated 7/28/2004 and 6/20/2005.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, as per claim 4, the transition from L0 to Recovery to L0 to Polling must be shown or the feature canceled from the claim. No new matter should be entered.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, as per claim 5, the transition from Polling Compliance to Loopback Exit to Detect Quiet must be shown or the feature canceled from the claim. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 17 is objected to because of the following informalities: The examiner requests correction of line 7 to recite, "... to point link, the link interface circuit includes ...".

5. Claim 21 is objected to because of the following informalities: The examiner requests correction of line 1 to recite, "... wherein the predefined bit of the register ...". Please not that there is also a rejection of this claim based on indefiniteness (below).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Line 9 of the claim assumes that the IC device is in "said measurement mode". But the *link only* was placed in measurement mode in the preceding limitation above. The examiner requires a clear statement or limitation that resolves which, of the IC device or link, is in measurement mode.

8. Claims 4, 5, 8 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims are rejected based on the same premise as claim 1 above.

9. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Line 4 recites the receive block as receiving "a stream of information", but the previous limitation above has already instantiated "a stream of information" on the point to point link. If the received information on the link is the same information as transmitted above, then the applicant is required to clearly state this in a limitation that is not indefinite. If the received information is not the same as the transmitted information, then the applicant is also required to clearly state such a difference.

10. Claim 11 recites the limitation "the same lane of the link" in line 3. There is insufficient antecedent basis for this limitation in the claim.

11. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Line 10 recites the receive block as receiving "a stream of information", but the previous limitation above has already instantiated "a stream of information" on the point to point link. If the received information on the link is the same information as transmitted above, then the applicant is required to clearly state this in a limitation that is not indefinite. If the received information is not the same as the transmitted information, then the applicant is also required to clearly state such a difference.

12. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Line 1 of the claim assumes that the MMC device is in "the measurement mode". But the *link only* was placed in measurement mode in the preceding limitation of claim 17 above. The examiner requires a clear statement or limitation that resolves which, of the MMC device or link, is in measurement mode.

13. Claim 20 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Line 2 recites the programming of "a predefined bit of a register of the IC device", but the previous limitation in claim 17 above has already programmed "a predefined bit of a register of the IC device". If the predefined bit is the same information as instantiated in claim 17 above, then the applicant is required to clearly state this in a limitation that is not indefinite.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1-3 and 6-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over "PCI Express Base Specification Revision 1.9" (herein Base Spec), in view of Jiang et al. (herein Jiang), US Patent No. 7127648.

As per claim 1:

The Base Spec teaches a method comprising: initializing a serial point to point link that communicatively couples an integrated circuit (IC) device to another IC device, by transferring a training sequence of symbols over the link (paragraph 4.2.4.1); programming a plurality of registers of the IC device (4.2.1) to i) set a test symbol data pattern (4.2.8) and ii) configure a lane transmitter for the link (4.2.5.3); programming a start bit in a register of the IC device, to request that the link be placed in a measurement mode (for example, use MSI Enable Bit, FIG. 7-8); and as best understood by the examiner (see 35 USC 112 rejection), and where the reference Base Spec fails to disclose specifically, the analogous art of Jiang further discloses the IC device (for example, compatible device of FIG. 6), in said measurement mode (test Mode in column 3), instructs said another IC device to enter a loopback mode for the link (for example, claim 33 of Jiang: "a configuration device for configuring the physical layer device under test to operate in loopback mode") in which symbols received over the link are looped back (column 3 lines 30-49), transmits a sequence of test symbols over the link and evaluates a looped back version of the sequence for errors (for example, the Abstract), wherein the sequence of test symbols have a data pattern (as per generator 625a, 625c of Jiang), and are transmitted (Abstract), as configured in the plurality of registers (the training sequence as in the Base Spec,4.2.8 or the generated

pattern from Jiang). And Jiang, in column 2, states advantages such as using an internal BIST to generate patterns to test a serial device at operational speeds. One with ordinary skill in the art at the time of the invention, would have found it obvious to include a operational speed BIST of Jiang with the PCI system of the Base Spec in order to effectively test such high speed data transfers as carried by PCI Express between devices.

As per claim 2:

The Base Spec further teaches the method of claim 1 wherein the initializing further comprises determining how many lanes are available for operation in said link (4.2.4.8.2). And in view of the motivation previously stated, the claim is rejected.

As per claim 3:

The Base Spec further teaches the method of claim 2 wherein the IC device indicates that the link is ready for normal operation with a determined number of lanes (4.2.4.8.2), and wherein the MSI enable of FIG. 7-8, the programming of the start bit is performed by a host while the link is ready for normal operation (for example, with MSI Enable, the device may be interrupted to perform user defined actions). And in view of the motivation previously stated, the claim is rejected.

As per claim 6:

The Base Spec further teaches the method of claim 1 further comprising: programming by a host a stop bit in a register of the IC device, to request that the link exits the measurement mode (5.8.4). And in view of the motivation previously stated, the claim is rejected.

As per claim 7:

The Base Spec further teaches the method of claim 6 wherein the programming of the start and stop bits include invoking PCI Express configuration write commands (2.2.3). And in view of the motivation previously stated, the claim is rejected.

As per claim 8:

The Base Spec further teaches the method of claim 1 wherein the IC device, in the measurement mode, instructs said another IC device to enter the loopback mode by transmitting a PCI Express TS1/TS2 Ordered Set over the link (4.2.4.1). And in view of the motivation previously stated, the claim is rejected.

As per claim 9:

Jiang teaches an integrated circuit (IC) device (FIG. 6) , comprising: an analog front end (AFE) transmit block to convert input symbols into a stream of information to be transmitted over a serial point to point link (FIG. 6 PMD Tx); an AFE receive block to receive a stream of information over the serial point to point link (FIG. 6 PMD Rx); and measurement mode circuitry (FIG. 6 625c) to provide the AFE transmit block a sequence of test symbols to be transmitted over the link while the link is operating in a measurement mode (FIG. 6 625c), the MMC to evaluate a sequence of test symbols, received by the AFE receive block over said link, for errors (FIG. 6 625e), but fails to further disclose that which the analogous art of the Base Spec discloses, wherein the link is to enter the measurement mode from a normal mode in response to a predefined bit of a register of the IC device being programmed (for example, use MSI Enable Bit, FIG. 7-8), the IC device having one or more programmable registers (Table 5-6) whose

bits instruct the MMC to change a data pattern in the sequence of test symbols and one of [a) an autoinvert setting, b) a default setting for an inverted lane of the link, c) an inversion setting, and] d) initial disparity (5.5.3.3), for the link. And in view of the motivation previously stated, the claim is rejected.

As per claim 10:

The Base Spec further discloses the IC device of claim 9 wherein the MMC is to log an error in the received sequence of test symbols in a software-accessible register of the IC device (5.5). And in view of the motivation previously stated, the claim is rejected.

As per claim 11:

The Base Spec further discloses the IC device of claim 9 wherein upon entering the measurement mode, the MMC is to instruct another IC device at another end of the link to loop the transmitted sequence of test symbols back over the same lane of the link (4.2.5.9). And in view of the motivation previously stated, the claim is rejected.

As per claim 12:

The Base Spec further discloses the IC device of claim 11 wherein the MMC is to provide a training sequence of symbols that is to be transmitted by the AFE transmit block upon the link entering the measurement mode and that is recognizable by said another IC device as including a request to place said another end of the link in a loopback mode (Table 4-2). And in view of the motivation previously stated, the claim is rejected.

As per claim 13:

The Base Spec further discloses the IC device of claim 11 wherein the MMC is to provide a PCI Express TS1/TS2 Ordered Set that is to be transmitted by the AFE transmit block upon the link entering the measurement mode and that includes a loopback bit being set (Table 4-2). And in view of the motivation previously stated, the claim is rejected.

As per claim 14:

The Base Spec further discloses the IC device of claim 9 wherein the sequence of test symbols includes a PCI Express SKP Ordered Set (4.2.4.1) followed by a compliance pattern (4.2.8). And in view of the motivation previously stated, the claim is rejected.

As per claim 15:

The Base Spec further discloses the IC device of claim 9 wherein the link is to remain in the measurement mode and is not to exit the measurement mode until a predefined bit of a register of the IC device has been programmed (4.2.8 where the exit is controlled by Electrical Idle Exit or Rest, last sentence of page 197). And in view of the motivation previously stated, the claim is rejected.

As per claim 16:

16. The IC device of claim 9 wherein the bit of the register is software-accessible during the normal mode via a configuration write command (2.2.3). And in view of the motivation previously stated, the claim is rejected.

As per claim 17:

The Base Spec teaches a system comprising: a processor (FIG. 1-2) CPU; a main memory (FIG. 1-2 Memory); and an integrated circuit (IC) device (FIG. 1-2 PCI Express Endpoint) which is communicatively coupled to the processor and the main memory and provides the processor with I/O access, the IC device (1.3.2) having link interface circuitry that supports a serial point to point link (1.3.2), the circuitry includes an analog front end (AFE) transmit block to convert input symbols into a stream of information to be transmitted over the link (4.2.1 and 4.2.1.1); an AFE receive block to receive a stream of information over the link (4.2.1 and 4.2.1.1); wherein the IC device having one or more programmable registers whose bits instruct the MMC to change a data pattern in the sequence of test symbols (see 4.2.1) and [one of a) an autoinvert setting, b) a default setting for an inverted lane of the link, c) an inversion setting, and d)] initial disparity (5.5.3.3), for the link, but fails to disclose features that the analogous art of Jiang further teaches, where Jiang discloses measurement mode circuitry (FIG. 6 625c) to provide the AFE transmit block a sequence of test symbols to be transmitted over the link while the link is operating in a measurement mode (FIG. 6 625c), the MMC to evaluate a sequence of test symbols, received by the AFE receive block over said link, for errors (FIG. 6 625e), and wherein the Base Spec further discloses that the link is to enter the measurement mode from a normal mode in response to a predefined bit of a register of the IC device being programmed (4.2.8 where the exit is controlled by Electrical Idle Exit or Rest, last sentence of page 197). And in view of the motivation previously stated, the claim is rejected.

As per claim 18:

The Base Spec further teaches the system of claim 17 wherein upon entering the measurement mode, the MMC is to instruct another IC device at another end of the link to loop the transmitted sequence of test symbols back over the same lane of the link (4.2.5.9). And in view of the motivation previously stated, the claim is rejected.

As per claim 19:

The Base Spec further teaches the system of claim 18 wherein the MMC is to provide a training sequence of symbols that is to be transmitted by the AFE transmit block upon the link entering the measurement mode and that is recognizable by said another IC device as including a request to place said another end of the link in a loopback mode (Table 4-2). And in view of the motivation previously stated, the claim is rejected.

As per claim 20:

The Base Spec further teaches the system of claim 17 wherein the link is to remain in the measurement mode and is not to exit the measurement mode until a predefined bit of a register of the IC device has been programmed (4.2.8 where the exit is controlled by Electrical Idle Exit or Rest, last sentence of page 197). And in view of the motivation previously stated, the claim is rejected.

As per claim 21:

The Base Spec further teaches the system of claim 17 wherein the bit of the register is software-accessible during the normal mode via a processor-initiated configuration write command (2.2.3). And in view of the motivation previously stated, the claim is rejected.

16. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over "PCI Express Base Specification Revision 1.9" (herein Base Spec), in view of Jiang et al. (herein Jiang), US Patent No. 7127648, and further in view of Hirose, US Patent Application Publiction No. 2004/0158675. As per claims 22 and 23, the memory controller hub and I/O controller hub of the claims 22 and 23 have not been claimed by the applicant as having a patentable distinction or feature that would distinguish the device from other devices. Instead, this application of state of the art hubs on serial links appears to be in the realm of design requirements in the practice of sound engineering principles, to connect with serial memories and I/O devices, rather than a unique circuit feature that would be patentable, and therefore represents a prima facie case of obviousness. The applicant's attention to Hirose is requested, where, for example, in FIG. 4, a memory controller hub and I/O controller hub are illustrated as design choice units, and are not represented as patentable features. Such a case of obviousness in a design choice renders the claims 22 and 23 rejected as a prim facie case of obviousness, with Hirose being such an example of a design choice.

Applicants can rebut a prima facie case of obviousness by showing the criticality of the claimed arrangement. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed.

Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results.

Allowable Subject Matter

17. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The transition from L0 to Recovery to L0 to Polling has not been disclosed by the references Base Spec nor Jiang, and therefore would be allowable as stated herein.

18. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The method of claim 1 wherein the IC device, upon exiting the measurement mode for the link, makes the following PCI Express state transitions: Polling Compliance to Loopback Exit to Detect Quiet has not been disclosed by the Base Spec and Jiang, and therefore would be allowable as stated herein.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/John P Trimmings/
Examiner, Art Unit 2117
1/10/2008

jpt

OK to enter. 1/9/08. JK

AMENDMENTS TO THE DRAWINGS

Applicants submit herewith ten (10) replacement drawing sheets (including FIGS. 1-3, 4A-4C and 5-9) to replace the informal drawings filed with the subject application on December 31, 2003. The Examiner should note that FIG. 9 has been amended for an obvious typographical error, amending the legend "Builing Switch" to "Building Switch".